High Efficiency Fast Response 10A, 23V Input Synchronous Step Down Regulator

General Description

The SY8270C develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 10A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. SY8270C also integrates a 100mA LDO with bypass switch.

The SY8270C operates over a wide input voltage range from 5.5V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor.

Ordering Information

SY8270 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8270CTMC	QFN3×4-13	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (top/bottom): 18/8mΩ
- Wide Input Voltage Range: 5.5-23V
- Integrated Bypass Switch: 1.5Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 0.8ms Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz.
- 10A Output Current Capability
- +/-1.5% Output Voltage Accuracy
- Power Good Indicator
- Output Discharge Function
- Output Current Limit Protection
- Output Under Voltage, Over Voltage Latch Off Protection
- Input UVLO
- Over Temperature Protection
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×4-13

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

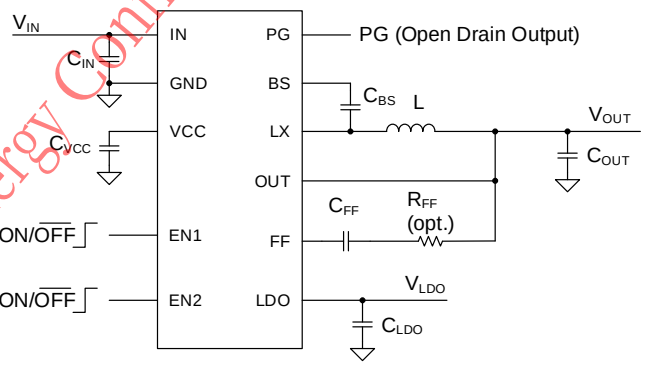


Figure1. Schematic Diagram

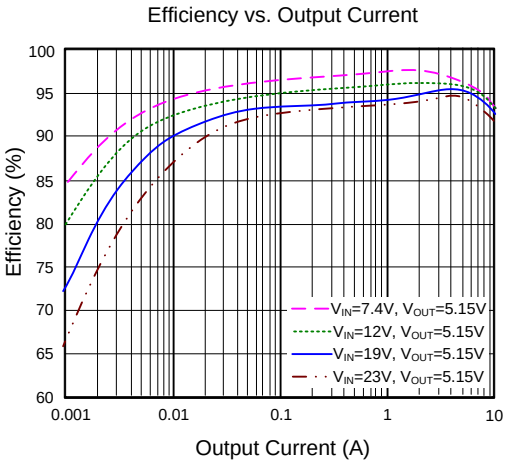
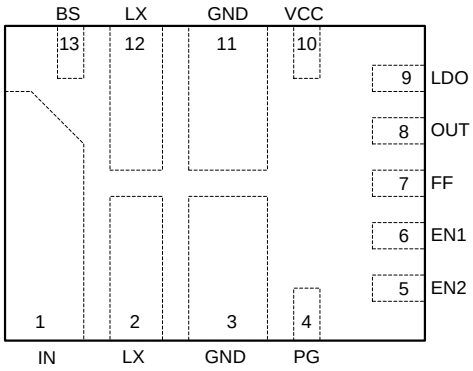


Figure2. Efficiency vs. Output Current

Pinout (top view)



(QFN3×4-13)

Top Mark: BTX***xyz***, **(**Device code: BTX, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	1	Input pin. Decouple this pin to GND pin with at least a 10μF ceramic cap.
LX	2,12	Inductor pin. Connect this pin to the switching node of inductor
GND	3,11	Ground pin.
PG	4	PG is an open-drain output pin. This pin is externally pulled high when the output voltage is within 92% to 120% of regulation voltage range. Otherwise, this pin is internally pulled low.
EN2	5	Enable control of the IC and internal LDO. Pull this pin high to turn on the IC and internal LDO. Do not leave this pin floating.
EN1	6	Enable control of the DC/DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating.
FF	7	Output feed forward pin. Connect RC network from the output to this pin.
OUT	8	Output pin. Connect to the output of DC/DC regulator. The pin also provides the bypass input for 5V LDO.
LDO	9	5V LDO output. Decouple this pin to ground with at least a 4.7μF capacitor.
VCC	10	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2μF ceramic capacitor.
BS	13	Boot-strap pin. Supply high side gate driver. Decouple this pin to LX pin with a 0.1μF ceramic capacitor.

Block Diagram

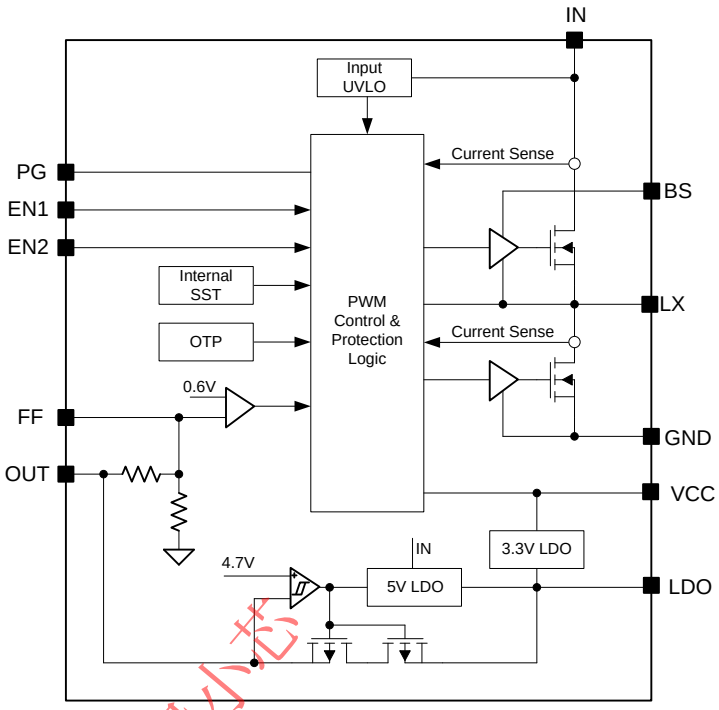


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX, PG ---------- 25V
BS-LX ---------- 4V
EN1, EN2 ---------- 25V
VCC ---------- 4V
LDO ---------- 6V
OUT ---------- 6V
FF ---------- 6V
Power Dissipation, P_D @ T_A = 25°C QFN3×4-13 ----------3.7W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 27°C/W
θ_{JC} ---------- 4.3°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 5.5V to 23V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 100µF, T_A = 25°C, I_{OUT} = 1A, unless otherwise specified)

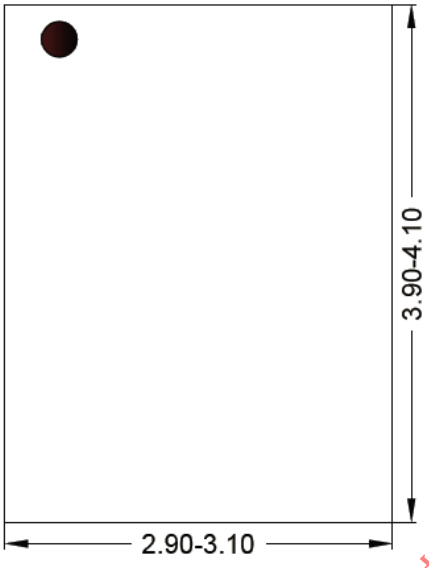
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		5.5		23	V
Quiescent Current	I_Q	EN1=EN2=1, I_{OUT}=0, V_{OUT}=V_{SET}×105%		110	145	µA
Shutdown Current 1	I_{SHDN1}	EN1=0, EN2=1		55	70	µA
Shutdown Current 2	I_{SHDN2}	EN1=0, EN2=0		6	10	µA
Output Voltage Setpoint	V_{SET}	CCM	5.07	5.15	5.23	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			18		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			8		mΩ
Output Discharge Current	I_{DIS}	V_{OUT}=5V		70		mA
Top FET Current Limit	$I_{LMT,TOP}$			20		A
Bottom FET Current Limit	$I_{LMT,BOT}$		11.5		16	A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%V_{SET}		0.8		ms
EN Input Voltage High	$V_{EN,H}$		1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
Input UVLO Threshold	V_{UVLO}				5	V
Input UVLO Hysteresis	V_{HYS}			0.2		V
Switching Frequency	F_{SW}	CCM	500	600	700	kHz
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			150		ns
VCC Output Voltage	V_{CC}	VCC with 1mA load	3.15	3.3	3.45	V
Output Over Voltage Threshold	V_{OVP}	V_{FB} Rising	115	120	125	%V_{REF}
Output OVP Delay	$V_{OVP,DLY}$			20		µs
Output Under Voltage Protection Threshold	V_{UVP}	V_{FB} falling	45	50	55	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			200		µs
Power Good Threshold	V_{PG}	V_{FB} rising (good)	80	84	88	%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$			2		%V_{REF}
Power Good Delay	$t_{PG,R}$	Low to high		200		µs
	$t_{PG,F}$	High to low		20		µs
LDO Output Voltage	V_{LDO}	V_{IN}=12V, no load	4.85	5	5.15	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=100mA		300		mV
LDO Output Current Limit	$I_{LMT,LDO}$		130		350	mA
Bypass Switch $R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.5		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		4.5	4.7	4.9	V
Bypass Switch Switchover Hysteresis	$V_{BYP,HYS}$			0.2		V
Bypass Switch OVP Threshold	$V_{BYP,OVP}$			120		%V_{LDO}
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

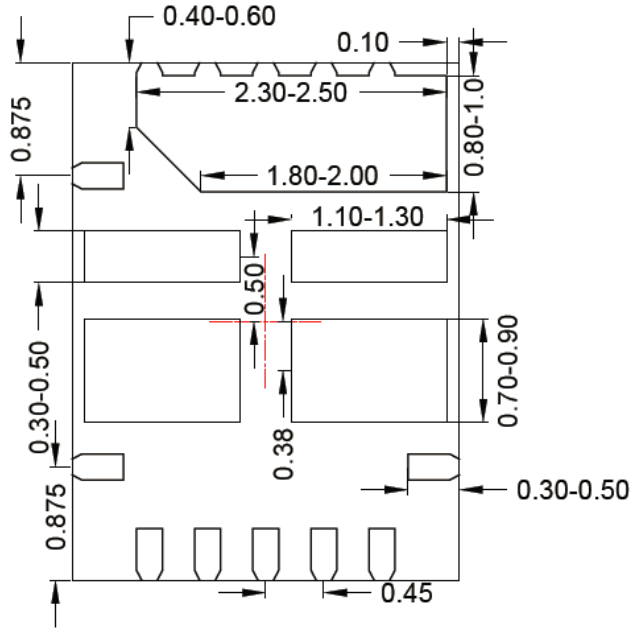
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

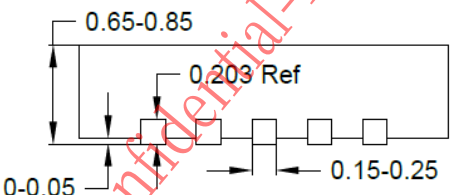
QFN3×4-13 Package Outline Drawing



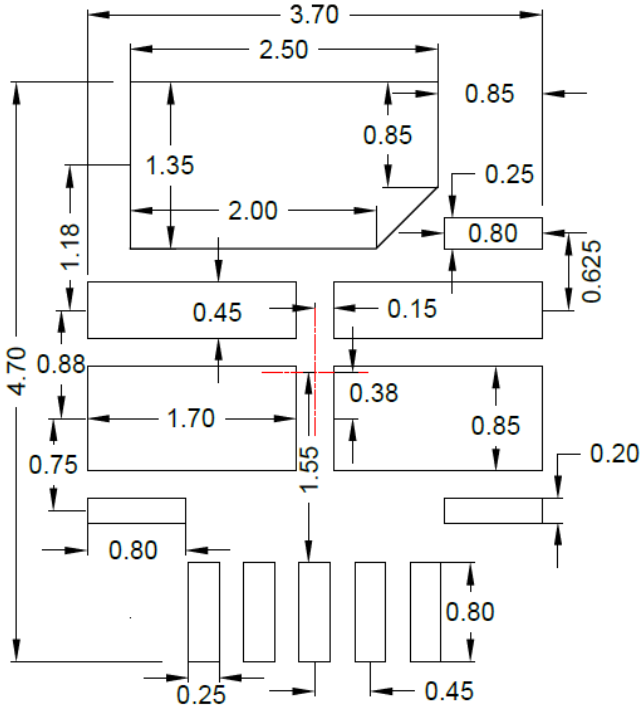
Top View



Bottom View



Front View

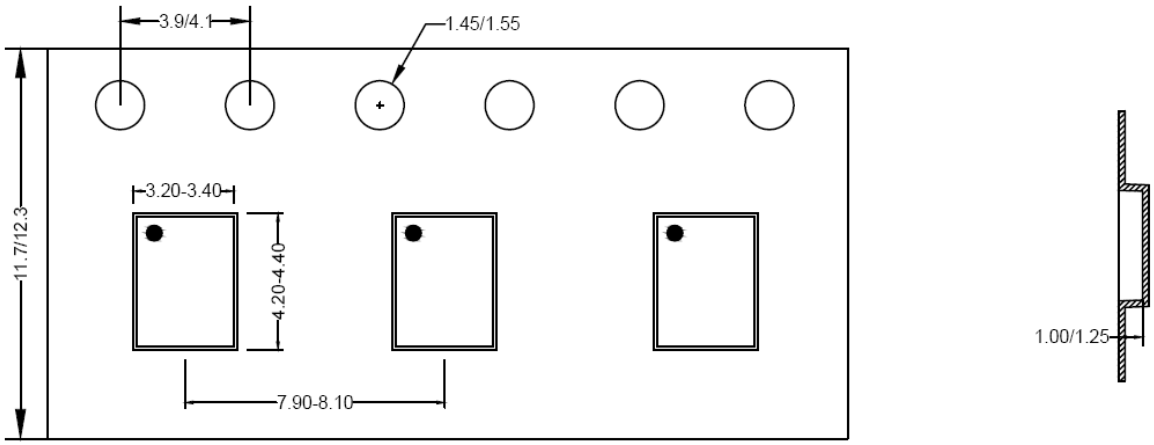


Recommended PCB layout
(Reference only)

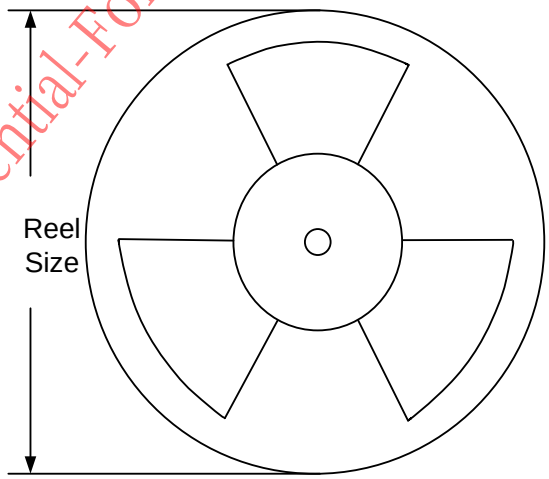
Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, center line on drawing refers to the chip body center

Taping & Reel Specification

1. QFN3×4-13 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA